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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,366	09/25/2003	Kenneth J. Goodnow	BUR920030028US1	2365

30449 7590 03/27/2006

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EXAMINER	
KRAVETS, LEONID	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,366	GOODNOW ET AL.	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Reference 50. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Paragraph 9 should be amended to read "electrically coupling each of said local memory structures [[is]] to each of the remaining local memory structures".

3. The system referred to in Paragraph 16, line 20 and 23 should be reference 3, not reference 7. This error occurs throughout the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-14, 16-19 and 21-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanenbaum (Distributed Operating Systems), and further in view of Pentkovski (US Pub No 2004/0039880).

As per claim 1, Tanenbaum discloses a ring based structure electrically connecting processor and memory units with each other. Tanenbaum does not disclose the plurality of systems within a single semiconductor device.

Pentkovski discloses a semiconductor device, comprising: a plurality of systems within the semiconductor device (Fig 4, Ref 400), each system comprising at least one processing device and a local memory structure (Fig 4, Ref 405, 410).

Tanenbaum and Pentkovski both further disclose the device wherein each said processing device is electrically coupled to each said local memory structure within each said system, wherein each said local memory structure is electrically coupled to each of the remaining local memory structures [Coupled through interface of Pentkovski (Fig 4, Ref 430); Coupled through ring architecture of Tanenbaum (Fig 6-5(a)].

Tanenbaum further discloses the device wherein each said local memory structure is adapted to share address space with each of said processing devices [A single address space is divided into a private part and a shared part (Page 298, Section 6.2.3, 1st Paragraph; Fig 6-5 (a))], and wherein each said processing device is adapted to transmit data and instructions to each said local memory structure (Page 300, 3rd Paragraph).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the chip multiprocessor system of Pentkovski into the system of Tanenbaum, since Tanenbaum and Pentkovski are from the same field of endeavor, namely multiprocessors and this would allow for improving the performance of the system by improving overall throughput (Pentkovski, Paragraphs 4-5).

As per claim 2, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each of the local memory structures in each said system comprises a first address space that is shared with the processing devices in the other systems and wherein each of the local memory structures in each said system comprises a second address space that is not shared with the processing devices in any of the other systems (Tanenbaum, Page 298, Section 6.2.3, 1st Paragraph, Lines 3-4).

As per claim 3, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each said processing device is further adapted to retrieve data and

instructions from each said local memory structure (Tanenbaum, Page 300, 3rd Paragraph).

As per claim 4, Pentkovski and Tanenbaum disclose the semiconductor device of claim 3, wherein each local memory structure comprises a memory device coupled to a memory control device, and wherein the memory control device is adapted to control a flow of said data and instructions between each processing device and each memory device [Tanenbaum discloses a memory management unit (Fig 6-5, (b))].

As per claim 6, Pentkovski and Tanenbaum disclose the semiconductor device of claim 4, wherein the memory device is selected from the group consisting of, random access memory, read only memory, and erasable programmable read only memory [Tanenbaum uses cache memories, which can be DRAM, a type or random access memory (Fig 6-5(b))].

As per claim 7, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each said system is adapted to transmit a memory write message to each of other said systems [Tanenbaum discloses transmitting a memory write message onto the ring topology, thus each system is adapted to transmit a memory write message to each of other said systems since the message will circulate around the ring (Page 300, Paragraphs 5-7).

As per claim 8, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each said local memory structure is electrically coupled to each of the remaining local memory structures with a high speed serial link [Each memory structure and processor is linked through the ring structure of Tanenbaum, and through an interface in Pentkovski (Tanenbaum Fig 6-5 (b); Pentkovski, Fig 4, Ref 430).

As per claim 9, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein a physical distance between each said processing device and each said local memory structure within each said system is in a range of about 50 microns to about 400 microns [It would be obvious to place the memory and processing device within a close distance of each other to speed up communication between the units. Tanenbaum shows such a structure in Fig 6-5(b)].

As per claim 10, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each said processing device is selected from the group consisting of a central processing unit and a digital signal processor (Tanenbaum, Fig 6-5(b)).

As per claim 11, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein the plurality of systems is adapted to maintain data coherency between each of said memory structures and each of said processing devices [Tables contain an entry for each block in the shared address space and each entry contains valid, exclusive, home and interrupt bits thus providing coherency between memory

structures and processing devices (Page 300, 1st Paragraph).

As per claim 12, Pentkovski and Tanenbaum disclose the semiconductor device of claim 11, wherein said data coherency is maintained using a protocol selected from the group consisting of contention, token passing, and polling [Tanenbaum discloses token passing within the ring network (Page 298, Section 6.2.3, 2nd Paragraph)].

As per claim 13, Pentkovski and Tanenbaum disclose the semiconductor device of claim 1, wherein each system comprises a plurality of processing devices electrically coupled to each said local memory structure within each said system [Ring topology of Tanenbaum provides for each processor being coupled to each memory device through the path of the ring (Fig 6-5(a,b)].

As per claim 14, Pentkovski and Tanenbaum disclose the semiconductor device of claim 13, wherein each local memory structure comprises a memory device coupled to a memory control device, and wherein the memory control device is adapted to control a flow of said data and instructions between each of the plurality of processing device and each memory device [Tanenbaum discloses a memory management unit (Fig 6-5, (b))].

As per claims 16-19, 21-29 please see rejection of claims 1-4, 6-14 above.

Allowable Subject Matter

6. Claims 5, 15, 20 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on Mon-Fri 8-430.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonid Kravets
Patent Examiner
Art Unit 2189

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

March 20, 2006